REMARKS

The present application was filed on May 25, 2001 with claims 1 through 35. Claims 1 through 35 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 1-5, 9, 10, 12-14, 17, 20, 21, 24, 27, 28, 31, 32, 34, and 35 under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. (United States Patent Number 6,490,654) in view of Bogin et al. (United States Patent Number 5,835,435), rejected claims 11, 12, 16, 23, 26, and 33 under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Bogin et al. and Fuller (United States Patent Number 5,632,038), rejected claims 15 and 25 under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Bogin et al. and Takahashi (United States Patent Number 6,345,336), and rejected claims 27-29 and 31-32 under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Stein et al., Session V: "Storage Array and Sense/Refresh Circuit for Single-Transistor Memory Cells," 1972, pages 56-57, and Fuller. The Examiner indicated that claims 6-8, 18, 19, 22, and 30 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Independent Claims 1, 20, 27 and 34

Independent claims 1, 20, 27, and 34 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Bogin et al. Regarding claim 1, the Examiner acknowledges that Wickeraad fails to teach "powering down cache lines if the cache lines had not been accessed in a predetermined time period," but asserts that Bogin teaches this limitation. (FIG. 7; col. 2, lines 44-47; col. 5, lines 21-49; and col. 9, lines 19-44.) Regarding claim 27, the Examiner asserts that Wickeraad discloses a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period (col. 1, lines 25-30; col. 3, lines 30-33; col. 4, lines 56-61).

Applicants note that Bogin teaches that "a separate clock enable signal is provided to each of a plurality of rows of SDRAM components in a system memory so that the rows may be powered or powered down independently of one another." (Col. 2, lines 44-47.) Bogin teaches that "a row of SDRAM components is said to be *powered when its clock enable signal is asserted*, and

powered down when its clock enable signal is deasserted." (Col. 5, lines 39-42; emphasis added.) Neither Wickeraad nor Bogin discloses or suggests that a timer is configured to ***remove power*** to an associated cache line. Independent claim 1 requires a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that *removes power* to said associated cache line after a decay interval. Independent claim 20 requires *removing power* from said associated cache line after a decay interval.

Thus, Wickeraad and Bogin, alone or in combination, do not disclose or suggest removing power from said associated cache line after a decay interval, as required by independent claims 1 and 20.

Regarding claim 27, Applicants note that the present disclosure defines a "safe period" as a period in which accessed cells are still reliable in regard to memory cell decay (page 10, lines 7-12). Neither Wickeraad nor Bogin discloses or suggests that a timer is configured to reset a valid bit associated with a cache line after a *safe period.* Independent claim 27 requires a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said *safe period.* Independent claim 34 requires resetting a valid bit associated with said cache line after said *safe period.*

Thus, Wickeraad and Bogin, alone or in combination, do not disclose or suggest resetting a valid bit associated with said cache line after said safe period, as required by independent claims 27 and 34.

Applicants also note that Bogin teaches that "if, while the bank is in the active state 89, no access requests are detected within a predetermined time, this lack of activity is detected decision block 94 and the bank is transitioned to precharge state 95 to close the open page in a precharge operation. After the precharge is completed, the bank returns to the idle state 85." (Col. 8, lines 35-40.) Thus, Bogin teaches that a *lack of activity causes the bank to return to the idle state.* Wickeraad teaches, however, "the cache lines *most likely to be needed soon are least likely to be replaced.*" (Col. 5, lines 19-20; emphasis added.) Thus, since Bogin and Wickeraad teach away from each other, a person of ordinary skill in the art would not look to combine Wickeraad and Bogin.

Additional Cited References

Fuller was cited by the Examiner for its disclosure of a dirty bit associated with each of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval. Applicants note that Fuller teaches that "the control and power management logic monitors the activity of the processor and automatically places the secondary cache memory into a low power mode (such as, for example, turning off the cache) during periods of inactivity." (Col. 3, lines 18-21.) Thus, Fuller teaches to turn off the *entire secondary cache* (*not a line of the cache*). Independent claim 1 requires a timer associated with *each of said plurality of cache lines*, each of said timers configured to control a signal that *removes power to said associated cache line* after a decay interval. Independent claim 20 requires resetting said timer each time said cache line is accessed; and removing power from said associated cache line after a decay interval.

In addition, Fuller actually teaches away from the present invention by teaching to base the decision to turn off the cache based on the inactivity of the processor (col. 3, lines 22-30). Independent claims 1 and 20 require removing power from an associated cache line after a decay interval.

Thus, Fuller does not disclose or suggest a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval, as required by independent claim 1, does not disclose or suggest resetting said timer each time said cache line is accessed; and removing power from said associated cache line after a decay interval, as required by independent claim 20, does not disclose or suggest that each of said timers controls a signal that resets a valid bit associated with said cache line after said safe period, as required by independent claim 27, and does not disclose or suggest resetting a valid bit associated with said cache line after said safe period, as required by independent claim 34.

Takahashi was also cited by the Examiner for its disclosure of a "first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line." Applicants note that Takahashi is directed to a method for reducing power consumption in the tag RAM of an instruction cache memory. (See, Abstract.)

Takahashi, however, does not address the issue of timers associated with cache lines.

Thus, Takahashi does not disclose or suggest a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval, as required by independent claim 1, does not disclose or suggest resetting said timer each time said cache line is accessed; and removing power from said associated cache line after a decay interval, as required by independent claim 20, does not disclose or suggest that each of said timers controls a signal that resets a valid bit associated with said cache line after said safe period, as required by independent claim 27, and does not disclose or suggest resetting a valid bit associated with said cache line after said safe period, as required by independent claim 34.

Stein et al. was also cited by the Examiner for its disclosure of one or more dynamic random memory access (DRAM) cells. Stein et al., however, do not address the issue of timers associated with cache lines.

Thus, Stein et al. do not disclose or suggest a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval, as required by independent claim 1, do not disclose or suggest resetting said timer each time said cache line is accessed; and removing power from said associated cache line after a decay interval, as required by independent claim 20, do not disclose or suggest that each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period, as required by independent claim 27, and do not disclose or suggest resetting a valid bit associated with said cache line after said safe period, as required by independent claim 34.

Dependent Claims 2-19, 21-26, 28-33 and 35

Dependent claims 2-5, 9, 10, 12-14, 17, 21, 24, 28, 31, 32, and 35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Bogin et al., claims 11, 12, 16, 23, 26, and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Bogin et al. and Fuller, claims 15 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of Bogin et al. and Takahashi, and claims 27-29 and 31-32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wickeraad et al. in view of

Stein et al. and Fuller.

Claims 2-19, 21-26, 28-33 and 35 are dependent on claims 1, 20, 27, and 34, respectively, and are therefore patentably distinguished over Wickeraad et al., Bogin et al., Fuller Takahashi, and Stein et al. (alone or in any combination) because of their dependency from independent claims 1, 20, 27, and 34 for the reasons set forth above, as well as other elements these claims add in combination to their base claim. The Examiner has already indicated that claims 6-8, 18, 19, 22, and 30 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

Kevin M. Mason

Date: April 20, 2005

Kevin M. Mason
Attorney for Applicant(s)
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560